

28. (Currently Amended) The multimedia interface according to claim ~~23~~ 59, further comprising a programmable memory interface (PMI) core incorporated on the IC chip.

29. (Previously Amended) Multimedia interface according to claim 37, wherein:
the at least one additional core includes the audio and/or video CODEC; and
the power-down circuitry provides the power and/or processing savings when the audio and/or video CODEC is not in use.

30. (Previously Amended) Multimedia interface according to claim 37, wherein:
the at least one additional core includes the PLL circuitry; and
the power-down circuitry provides the power and/or processing savings when the PLL circuitry is not in use.

31. (Previously Amended) Multimedia interface according to claim 37, wherein:
the at least one additional core includes the serial interface core; and
the power-down circuitry provides the power and/or processing savings when the serial interface core is not in use.

32. (Previously Amended) Multimedia interface according to claim 31, wherein:
the serial interface core is incorporated within the reconfigurable logic block.

33. (Previously Amended) Multimedia interface according to claim 37, wherein:
the at least one additional core includes the programmable CPU interface core;
and
the power-down circuitry provides the power and/or processing savings when the programmable CPU interface core is not in use.

34. (pending) Multimedia interface according to claim 33, wherein:
the programmable CPU interface core is incorporated within the reconfigurable logic block.

35. (pending) Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a media processor block incorporated on the IC chip; and
a programmable memory interface (PMI) core incorporated on the IC chip, the
PMI core communicates with off-chip memory and configures it virtually into what is optimal
for an application that demands non-standard size memory.

36. (pending) Multimedia interface according to claim 52, wherein:
the programmable memory interface core is incorporated within the
reconfigurable logic block.

37. (pending) Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a media processor block incorporated on the IC chip; and
at least one additional core selected from the group consisting of
audio and/or video CODECs for interfacing to external analog signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the
IC chip;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
further comprising power-down circuitry, in combination with one or more of these
additional cores, incorporated on the IC chip to provide power and/or processing savings when a
given one of the cores is not in use. (no change)

38. (Previously Amended) Signal processing interface according to claim 46,
wherein:
the at least one additional core includes the audio and/or video CODEC; and
the power-down circuitry provides the power and/or processing savings when the

audio and/or video CODEC is not in use.

39. (Previously Amended) Signal processing interface according to claim 46,
wherein:

the at least one additional core includes the PLL circuitry; and
the power-down circuitry provides the power and/or processing savings when the
PLL circuitry is not in use.

40. (Previously Amended) Signal processing interface according to claim 46,
wherein:

the at least one additional core includes the serial interface core; and
the power-down circuitry provides the power and/or processing savings when the
serial interface core is not in use.

41. (Previously Amended) Signal processing interface according to claim 40,
wherein:

the serial interface core is incorporated within the reconfigurable logic block.

42. (Previously Amended) Signal processing interface according to claim 46,
wherein:

the at least one additional core includes the programmable CPU interface core;
and
the power-down circuitry provides the power and/or processing savings when the
programmable CPU interface core is not in use.

43. (Pending) Signal processing interface according to claim 42, wherein:
the programmable CPU interface core is incorporated within the reconfigurable
logic block.

44. (Pending) Signal processing interface, comprising:
an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;
a RISC core incorporated on the IC chip; and
a programmable memory interface (PMI) core incorporated on the IC chip, the PMI core communicates with off-chip memory and configures it virtually into what is optimal for an application that demands non-standard size memory.

45. (Pending) Signal processing interface according to claim 58, wherein:
the programmable memory interface core is incorporated within the reconfigurable logic block.

46. (Pending) Signal processing interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a RISC core incorporated on the IC chip; and
at least one additional core selected from the group consisting of
audio and/or video CODEC for interfacing to external analog signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

47. (currently amended) The multimedia interface according to claim ~~23~~ 59, further comprising a configuration port that allows a user access to the block of reconfigurable logic from off-chip.

48. (Pending) Multimedia interface, comprising:
an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;
a media processor block incorporated on the IC chip; and
audio and/or video CODEC and an analog interface incorporated on the IC chip,
the audio and/or video CODEC communicating, via the analog interface, with external analog
signals.

49. (Canceled) ~~Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a media processor block incorporated on the IC chip;
means, incorporated on the IC chip, for reducing skew within various blocks
within the IC chip; and
further comprising power down circuitry incorporated on the IC chip to provide
power and/or processing saving when the means for reducing skew is not in use.~~

50. (Canceled) ~~The multimedia interface according to claim 31, wherein the serial
interface standard is one of USB and IEEE 1394.~~

51. (Canceled) ~~The multimedia interface according to claim 32, wherein the serial
interface standard is one of USB and IEEE 1394.~~

52. (previously amended) Multimedia interface according to claim 37, wherein:
the at least one additional core includes the PMI core; and
the power-down circuitry provides the power and/or processing savings when the
PMI core is not in use.

53. (Pending) The multimedia interface according to claim 37, wherein the media
processor has a virtual instruction set capable of implementing a variety of multimedia
algorithms.

54. (Pending) Signal processing interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a RISC core incorporated on the IC chip; and
audio and/or video CODEC and an analog interface incorporated on the IC chip,

the audio and/or video CODEC communicating, via the analog interface, with external analog signals.

55. ~~(Canceled) Signal processing interface, comprising:~~
~~an integrated circuit (IC) chip;~~
~~a block of reconfigurable logic incorporated on the IC chip;~~
~~a RISC core incorporated on the IC chip;~~
~~means, incorporated on the IC chip, for reducing skew within various blocks within the IC chip; and~~
~~further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing saving when the means for reducing skew is not in use.~~

56. ~~(Canceled) The signal processing interface according to claim 40, wherein the serial interface standard is one of USB and IEEE 1394.~~

57. ~~(Canceled) The signal processing interface according to claim 41, wherein the serial communication standard is one of USB and IEEE 1394.~~

58. (previously amended) Signal processing interface according to claim 46, wherein:
the at least one additional core includes the PMI core; and
the power-down circuitry provides the power and/or processing savings when the PMI core is not in use.

59. (currently amended) Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip; and
a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms incorporated on the IC chip separately from the reconfigurable logic block;
~~The multimedia interface according to claim 23,~~
wherein the block of reconfigurable logic contains a least common denomination set of instruction for operating the block of media processor.